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A new multilevel inverter topology based on switched-capacitor technique

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ABSTRACT

This paper presents a new multilevel inverter based on the switched-capacitor technique. The topology aims for renewable energy and fuel cell applications that demand high magnitude output ac voltage. This configuration of the inverter can produce a total of thirteen voltage levels using a single DC source. The topology features voltage boosting with a triple gain of the input voltage source without utilizing a boost DC-DC converter. Furthermore, the voltages of the capacitors are self-balanced at any desired voltage level during each cycle. Therefore, auxiliary circuits are no longer needed. A comparative study of the presented inverter with the classical topologies and recently introduced topologies has been done in power switches, driver circuits, blocking voltage of the switches, and boosting the input voltage. A simple fundamental switching scheme is applied to the proposed topology to validate the viability of the topology.

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1. INTRODUCTION

Multilevel inverters (MLIs) have become very popular and globally recognized for numerous industrial applications such as renewable energy systems, motor drives, Induction heating, electric vehicles, FACTs devices, active power filtering, and many more. MLIs possess numerous advantages compared to classical two-level inverters, such as decreased total harmonic distortion (THD), lower voltage stress across switches, and electromagnetic interference (EMI). The basic principle of MLIs is to generate a staircase voltage waveform near to sinusoidal with high power quality. The desired staircase voltage waveform is synthesized using an appropriate combination of different switches, reducing power switches' voltage stress and total harmonic distortion (THD) [1]-[4].

Generally, well-established classical MLIs are categorized into the following three main types: Cascaded H-Bridge (CHB), Neutral-Point Clamped (NPC), and Flying-Capacitor (FC). NPC MLIs are widely used in the industry. However, high-level NPC inverter structures require several clamping diodes and capacitors' balancing involving auxiliary circuits and sensors, making the system more complicated, less reliable, and more costly to maintain. The FC MLI is another inverter topology with an energy storage facility. The flying capacitors' voltage can be maintained at their respective levels using the topology's switching state redundancies. Thus, the voltage balancing mechanism becomes complicated. It is the prerequisite of too many bulky flying capacitors, and the complex control mechanism for capacitors balancing that limits higher levels on this inverter. The CHB MLIs, on the other hand, consists of several H-

bridge cells to produce multilevel output. However, these CHB MLIs are constructed using multiple isolated power sources, which somehow not suitable in many applications such as electric vehicle drives. Moreover, they generally employ more power switches, gate drives and resulting in more power losses. These issues motivate researchers to develop new inverter topologies, and to date, many inverter structures addressing those issues have been introduced in the literature[5]-[15].

Recent MLI topologies [5]-[15] tend to focus on increasing the efficiency and modularity of the MLIs. Hence, most of them have a more straightforward structure [3], but they are buck-type MLIs. They are not able to boost up the output voltage. Typically, a front-end DC-DC boost converter is required, which leading to complex control and structures. The boosting of input voltage should be the essential feature for the inverter topologies used for high voltage and renewable energy systems (RES). One such type of MLIs topologies is the switched capacitor (SC) based MLIs. In general, SC-MLIs contain a single DC source connected in various capacitors' configurations to boost the low input voltage.

Moreover, without any auxiliary circuits, the capacitor's voltage is self-balanced in SC-MLIs [16]. The boosting voltage ability and non-auxiliary circuits for balancing the capacitor voltage are remarkable benefits provided by these SC-MLIs. However, the existing SC-MLIs topologies consisted of many power switches and capacitors with high voltage stress; thus, the overall system becomes problematic, costly with high power losses. Hence, research on developing new SC-based MLIs to use fewer switches and capacitors with low voltage stress progresses [16]-[38].

SC-MLIs presented in [16]-[20] use a back-end H-bridge circuit for polarity change. This inverter exhibits a simple structure with a high number of voltage levels. However, four power switches in those structures must withstand high voltage stress equal to the load's peak voltage. It put limitations on these topologies for higher voltage applications. Other SC-MLI were proposed in the literature [39-41]. They require two switches only to withstand the blocking voltage equal to the peak output voltage. However, the voltage blocking rating is still regarded as high.

In this paper, a new SC-MLI topology is proposed. The advantages of the proposed SC-MLI topology include; 1. self-voltage balancing of capacitors without using auxiliary circuits and sensors; 2. Input voltage can boost with a gain of three; 3. a single DC source to generate multiple output voltage levels and 4. low voltage rated power switches. The total standing voltage (TSV) of the SC-MLI will be shown to be at the low side even though fewer components are employed. The design of the proposed SC-MLI will be elaborated on in the following sections. A simple fundamental switching scheme is used for the proposed SC-MLI to generate the 13-level output voltage. Simulation using Matlab-Simulink® software will be performed using different loading. From the results, it will be shown that the design of the proposed SC-MLI is validated.

2. THE PROPOSED MULTILEVEL INVERTER

The configuration of the proposed inverter topology is depicted in Figure 1. The topology consists of 11 unidirectional switches, a bidirectional switch (S_{11}), a diode, and three switched capacitors. With this inverter configuration, thirteen voltage levels can be achieved. The voltage of switched capacitor C_1 is balanced at a voltage level equal to Vin input voltage. Simultaneously, the input DC source of magnitude V_{in} charges switched capacitors C_2 and C_3 to the voltage level of 0.5Vin. As the capacitor's voltages are self-balancing in nature, sensors and auxiliary circuits are not required to balance switched capacitors in the presented inverter topology. Figure 2 depicts the pulses to generate a 13-level output voltage.

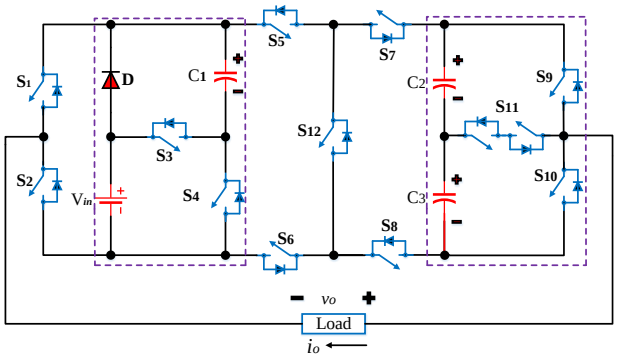


Figure 1. Proposed boost MLI circuit

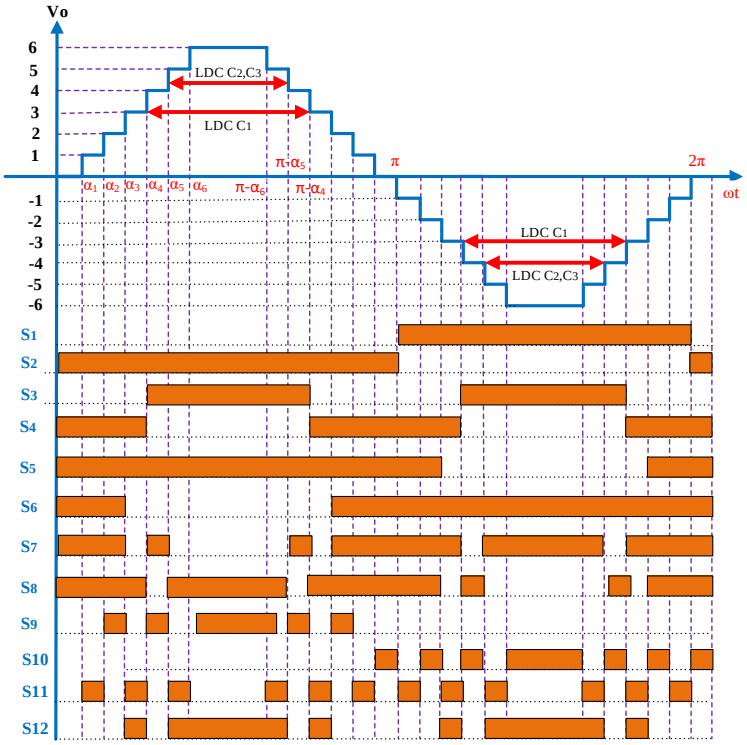


Figure 2. 13-level output voltage waveform and required pulses for switches

2.1. Modes of Operation

In this Section 2.1, the modes of operations that provide the basic principle of generating different voltage levels across the load are presented. The proposed SC-MLI operation modes in positive and negative half-cycles are shown in Figures 3 and 4, respectively. Table 1 shows all the switching states of the proposed SC-MLI. Here '1' and '0' represent on and off states of the switches, respectively. The charging state, discharging, and no-effect state of the switched capacitors are represented by 'C', 'D', and 'N', respectively. The upward arrow sign '↑' *shows the charging of switched capacitors while the downward sign '↓' shows the discharging of switched capacitors. The blue dotted line shows the path for charging of switched capacitors, while the red dotted lines show the direction of load current. The following paragraphs explain the mode of operation of the proposed SC-MLI in generating different output levels.*

$\pm 0.5V_{in}$ Voltage level: As shown in Figure 3(a), the switches S_2, S_6, S_8, and S_{11} are turned on to produce voltage level $0.5V_{in}$. Switch S_4 is turned on; thus, the diode is in forwarding conduction mode. The switched capacitor C_1 is parallel with the input DC source and charges it to V_{in} magnitude. The switched capacitors C_2 and C_3 are also parallel with input DC when switches S_5 and S_7 are turned on. It charges these capacitors to the voltage level of $0.5V_{in}$. To produce a voltage level of $-0.5V_{in}$, the switches S_1, S_5, S_7, and S_{11} are turned on, as shown in Figure 4(a). The process of charging the switched capacitors will remain the same as in the $0.5V_{in}$ state.

$\pm 1V_{in}$ Voltage level: As shown in Figure 3(b), the switches S_2, S_6, S_8, and S_9 are turned on to produce voltage level $1V_{in}$. The switched capacitor C_1 is parallel with the input DC source through S_4 and the diode. The capacitor charges to V_{in} magnitude. The switched capacitors C_2 and C_3 are also in parallel combination with input DC when switches S_6 and S_8 are turned on. It charges these capacitors to the voltage level of $0.5V_{in}$. To produce voltage level $-1V_{in}$, the switches S_1, S_6, S_8, and S_{10} are turned on, as shown in Figure 4(b). The process of charging the switched capacitors will remain the same as in the $1V_{in}$ state.

$\pm 1.5V_{in}$ Voltage level: As shown in Figure 3(c), the switches S_2, S_5, S_8, S_{11}, and S_{12} are turned on to produce voltage level $1.5V_{in}$. The switched capacitors C_3 is in series combination with input source and discharges. At that moment, there is no effect on capacitor C_2 in this state. Switch S_4 is turned on; thus, the diode is in forward conduction mode. The switched capacitor C_1 is parallel with the input DC source and charges it to the magnitude of $1V_{in}$. To produce voltage level $-1.5V_{in}$, the switches S_1, S_6, S_7 S_{11}, and S_{12} are turned on as shown in Figure 4(c). The process of charging the switched capacitors will remain the same as in the $0.5V_{in}$ state. In this state, C_3 provides the power to load in series combination with input source and discharges, while C_2 remains not affected.

Table 1. Switching states of the 13-level inverter

levels	Power switches												Capacitors			
	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	S_{11}	S_{12}	C_1	C_2	C_3	V_o
1	0	1	0	1	1	1	1	1	0	0	1	0	C	C	C	**$0.5V_{in}$**
2	0	1	0	1	1	1	1	1	1	0	0	0	C	C	C	**$1V_{in}$**
3	0	1	0	1	1	0	0	1	0	0	1	1	C	N	D	**$1.5V_{in}$**
4	0	1	1	0	1	0	1	0	1	0	0	0	D	N	N	**$2V_{in}$**
5	0	1	1	0	1	0	0	1	0	0	1	1	D	N	D	**$2.5V_{in}$**
6	0	1	1	0	1	0	0	1	1	0	0	1	D	D	D	**$3V_{DC}$**
0	0	1	0	1	1	1	1	1	0	1	0	0	C	C	C	**0**
-1	1	0	0	1	1	1	1	1	0	0	1	0	C	C	C	**$-0.5V_{in}$**
-2	1	0	0	1	1	1	1	1	0	1	0	0	C	C	C	**$-1V_{in}$**
-3	1	0	0	1	0	1	1	0	0	0	1	1	C	D	N	**$-1.5V_{in}$**
-4	1	0	1	0	0	1	0	1	0	1	0	0	D	N	N	**$-2V_{in}$**
-5	1	0	1	0	0	1	1	0	0	0	1	1	D	D	N	**$-2.5V_{in}$**
-6	1	0	1	0	0	1	1	0	0	1	0	1	D	D	D	**$-3V_{in}$**

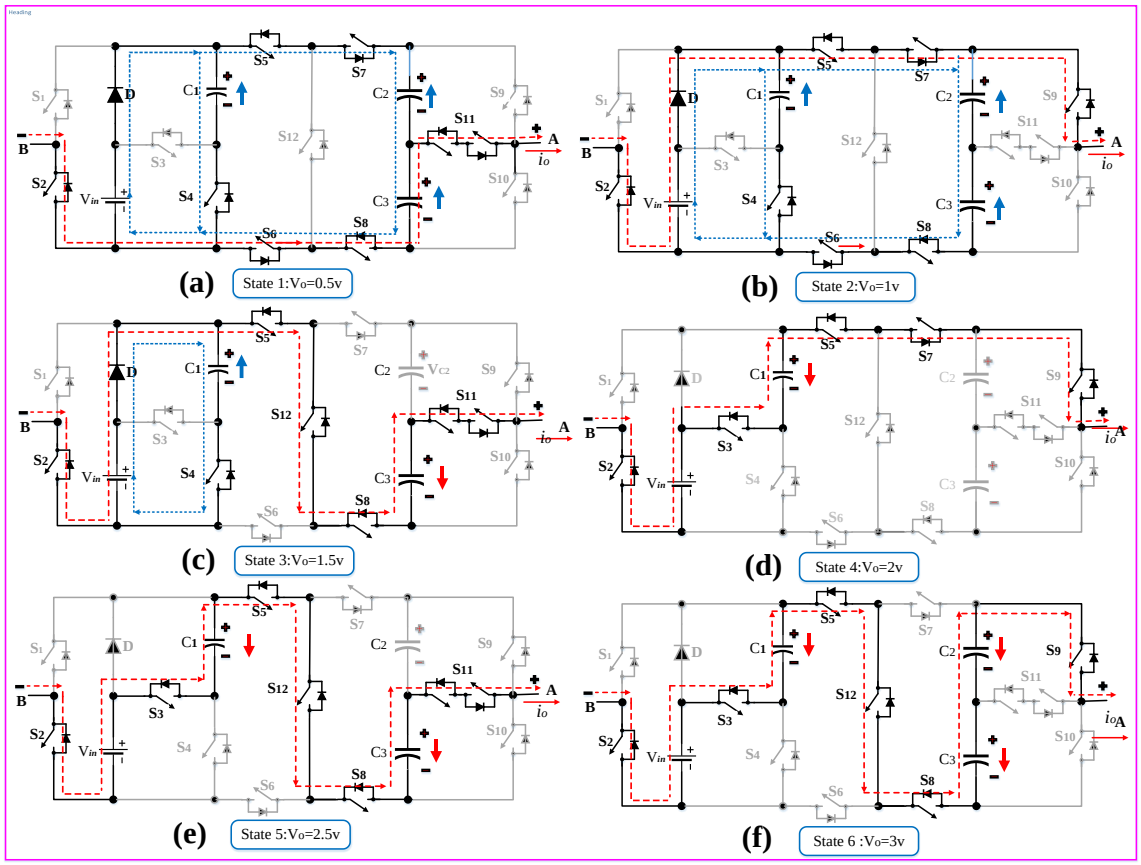


Figure 3. Operating modes of inverter during the positive half cycle

$\pm 2V_{in}$ Voltage level: As shown in Figure 3(d), the switches S_2, S_3, S_5, S_7, and S_9 are turned on to produce voltage level $+2V_{in}$. The switched capacitors C_1 is in series combination with the input source to provide the load current and discharges. Simultaneously, there is no effect on capacitors C_2 and C_3 in this mode of operation. To produce voltage level $-2V_{in}$, the switches S_1, S_3, S_6 S_8, and S_{10} are turned on as shown in Figure 4(d). The switched capacitors C_1 discharge as they come in series with the input source. At the same time, there is no effect on capacitors C_2 and C_3 in this state.

$\pm 2.5V_{in}$ Voltage level: As shown in Figure 3(e), to generate the voltage level $+2V_{in}$, the switches S_2, S_3, S_5, S_8 S_{11}, and S_{12} are turned ON. The switched capacitors C_1 and C_3 are combined with the input source to provide the load current and discharges. At the same time, there is no effect on capacitors C_3 in this mode of

operation. While in voltage level -2V_{in}, the switched capacitors C_1 and C_2 discharge as they come in series with the input source. The capacitors C_2 remains unaffected in this state.

±3V_{in} Voltage level: As shown in Figure. 3(f), in this mode of operation to produce voltage level ±3V_{in}, all the switched capacitors C_1, C_2 and C_3 are combined with the input source to provide the load current and therefore discharges.

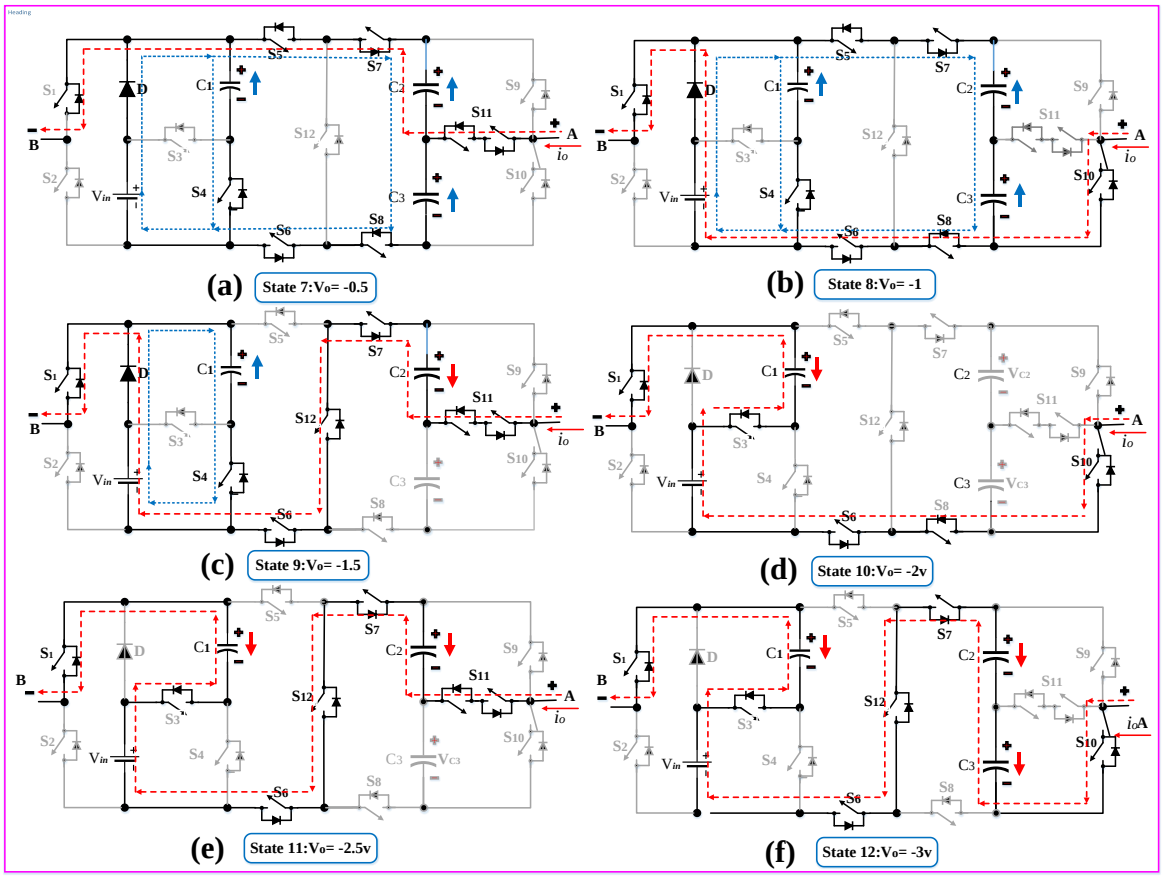


Figure 4. Operating modes of inverter during the negative half cycle

2.2. Modulation technique and Capacitor Value Calculation

In this paper, the fundamental switching frequency method is used to generate pulses for all the switches. A sinusoidal 50 Hz reference signal is compared with some available DC-voltage levels and generates related pulses for power switches. This switching technique's main advantage is low switching frequency, which significantly reduces the switching losses. Details of the fundamental switching frequency technique are not discussed here.

Generally, the switching angles θ_i can be obtained as (1)

$$\theta_i = sin^{-1}\left(\frac{2i-1}{N_l}\right),\ i=1, 2, 3, \ldots, \frac{N_l-1}{2} \quad (1)$$

In switched capacitor MLIs, the capacitor's optimum calculation is one of the most critical issues to retain the capacitor's voltage ripples in an acceptable range. For calculating capacitors' capacitance, the longest discharging cycle (LDC) for each capacitor over a complete output voltage cycle is considered. The capacitor discharges the maximum amount of charge during LDC. The value of discharging charge is dependent on the output current and LDC duration.

Therefore, the maximum discharging amount of the capacitor's charge is obtained by (2) and (3)

$$\Delta Q_1 = \frac{1}{2\pi f_0}\int_{\theta_4}^{\pi-\theta_4} I_o\, d\omega t \quad (2)$$

$$\Delta Q_{2,3} = \frac{1}{2\pi f_0}\int_{\theta_5}^{\pi-\theta_5} I_o \, d\omega t \quad (3)$$

Where, f_0 is the frequency of output waveform, I_o is the amplitude of load current, and ω is the corresponding angular frequency. Whereas, $[\theta_4, \pi-\theta_4]$ is the longest discharging cycle (LDC) of the capacitor C_1 and $[\theta_5, \pi-\theta_5]$ is the LDC interval of the capacitor C_2 and C_3. Thus, by assuming ΔV as the maximum allowable voltage ripple over the capacitor, the optimum capacitance values of switched capacitors can be calculated by (4) and (5)

$$C_1 = \frac{\Delta Q_1}{\Delta V} = \frac{1}{\Delta V}\frac{1}{2\pi f_0}\int_{\theta_4}^{\pi-\theta_4} I_o \, d\omega t \quad (4)$$

$$C_{2,3} = \frac{\Delta Q_{2,3}}{\Delta V} = \frac{1}{\Delta V}\frac{1}{2\pi f_0}\int_{\theta_5}^{\pi-\theta_5} I_o \, d\omega t \quad (5)$$

2.3. Comparatives study

Table. 2 presents the comparison study with other recently introduced MLIs, considering the capability of voltage boosting and self-balancing of switched capacitors. For generating 13-level voltage, the proposed SC-MLI topology requires the least component counts in power switches and gate drives. Moreover, it is achieved using a single DC source. The other topologies require more switches to attain the same voltage levels. The voltage stress across the power switches in the proposed topology is much lower than the rest topologies. It is clear from the comparison that the proposed topology requires the least number of power switches and blocking voltage compared to other inverter structures. Please be noted that TSV is defined as Total Standing Voltage, which is similar to the total voltage value that needs to be blocked by the power switch during its off state.

Table 2. Comparative analysis with other recently introduced SCMLIs

	[32]	[19]	[16]	[20]	[34]	Proposed
Levels	13	9	13	13	9	13
switches	29	10	16	14	12	13
driver	29	8	16	14	10	12
capacitors	5	2	4	4	2	3
sources	1	1	2	2	1	1
(TSV)*V_{in}	29	24	34	78	22	13.5

3. RESULTS AND DISCUSSION

Simulations are carried out using the Matlab-Simulink® computer software tool. A single-phase 13-level inverter was developed for simulation purposes with different parameters used as tabulated in Table 3. In this work, the fundamental frequency switching method is employed to generate the required gating pulse for the power switches. The selected input voltage source is 100V for simulation purposes, and the resistive load of 150 Ω and the inductive load of 150 Ω and 100m H are used for the proposed SC-MLI. Figures 5(a-b) illustrates the output voltage and current waveforms for the proposed SC-MLI. The output voltage and current have a peak of 297.5 V and 1.9 A, respectively. The voltage is boosted triple times from the 100 V input voltage value. It proves the viability of the proposed SC-MLI. The result with inductive load also confirms the capability of the proposed SC-MLI to operates with bi-directional capabilities.

Table 3. Parameters used for the simulation study

Parameters	value
Input voltage	100 V
Capacitances	C_1=1200 µF C_{l1}, $C_{l,2}$=1000 µF
Modulation indices	M_a=1, M_a=0.7
Output frequency	50 Hz
Input frequency	50 Hz
Load	150 Ω, 100m H

As depicted in Figure 5(c-d), the harmonic spectrum of the output voltage contains 4.65 % THD without using filters, while the harmonic spectrum of sinusoidal output current is having 2.53 % THD. All the obtained results satisfy the harmonics IEEE standards, i.e., IEEE519. The 13 levels at the output with

triple voltage gain and inductive load ability are validated through simulations. The current stress of the power switches is shown in Figure6 (a). By considering a 10 % voltage ripple, the optimum value of capacitor C_1 obtained is approximately 1200 µF and 1000 µF for capacitors of C_2 and C_3.

The switched capacitors voltages at the rated output and current waveforms are shown in Figure 7. The capacitor voltage of C_1 is maintained at 100 V, while C_2 and C_3 are maintained at 50 V, respectively. The result verifies the self-balancing of all three switched capacitors. The voltage ripples of the capacitors can also be observed. The maximum voltage ripples of C_1 are about 9 V, while capacitors C_2 and C_3 are around 8 V. The blocking voltage of each switch in the inverter is shown in Figure 6(b).

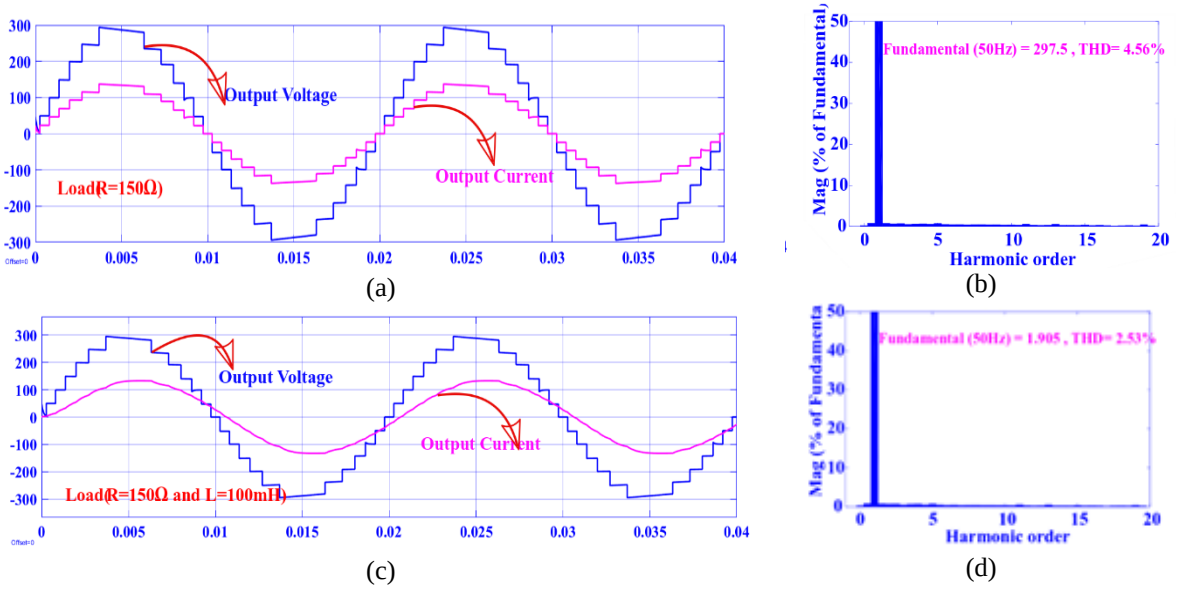


Figure 5. Output voltage and current waveforms, (a) resistive load, (b) inductive load, Harmonic spectrums, (c) output voltage, (d) current

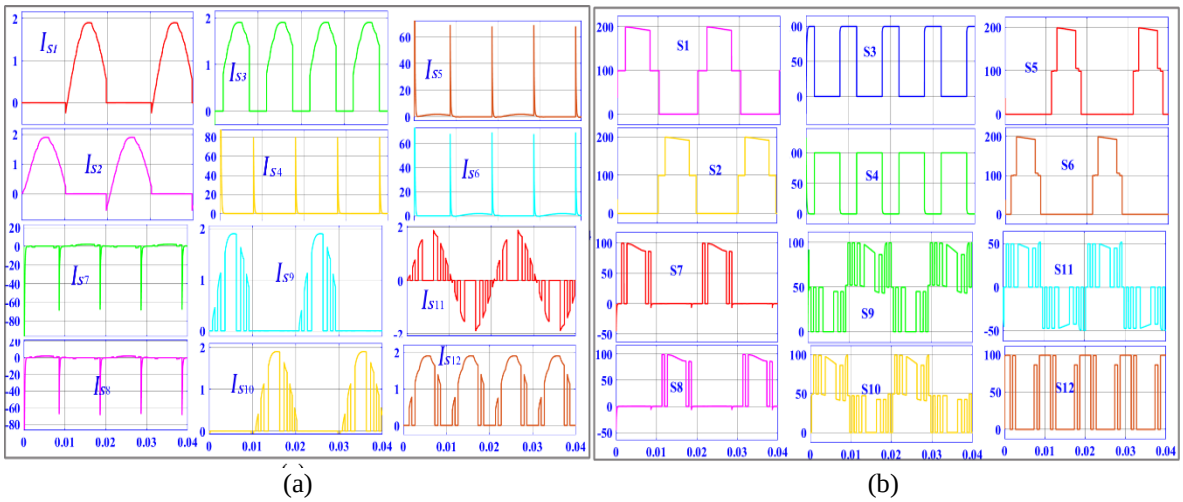
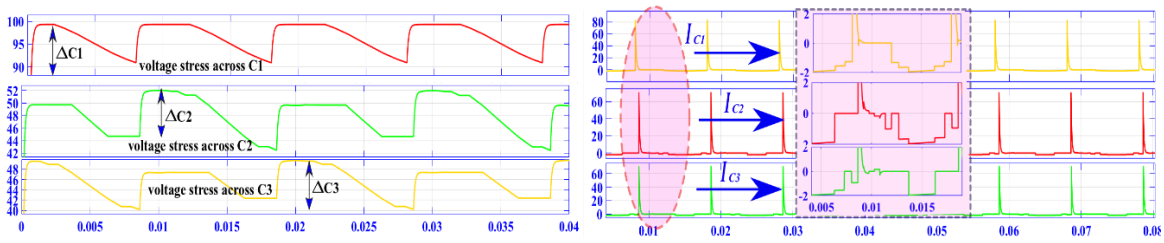


Figure 6. (a) Current through power switches, (b) Blocked voltages across power switches



(a) (b)

Figure 7. Voltage and current waveforms of the capacitors (V_{c1} $V_{c2,}$ and V_{c3})

4. CONCLUSION

This paper has proposed a new SC-MLI based on the switched-capacitor technique. The inverter has the capability of triple-voltage boosting and self-voltage balancing of switched capacitors. The working principle and different modes of operation with switched capacitors and their charging-discharging cycles have been addressed. This proposed SC-MLI generates a 13-level output voltage waveform by employing only a single input source. The voltage stress across the power switches is also proven to be on the low side. Simulations results with the 13-level inverter topology at different load conditions were obtained. Comparative study of the proposed SC-MLI with other inverter topologies shows the superiority of the proposed topology in reducing the number of power switches, the voltage stress on switches, size, and cost of the inverter system.

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